EEL 4744

Menu

- D-to-A (digital to analog) system on the XMEGA

D-to-A = DAC = D/A = D2A

See examples on web-site:
doc8331, doc8033

1

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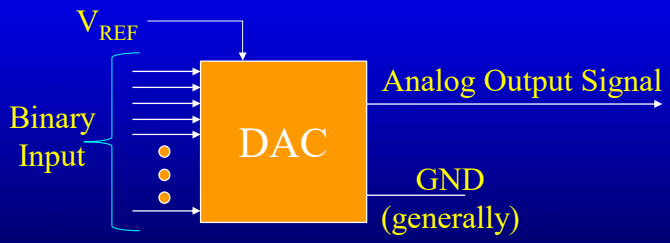
Digital to Analog Converters

- Digital to Analog Converter
  - > Also know as D-to-A, D/A, or DAC or as an Digital-to-Analog Converter (or a D2A)



2

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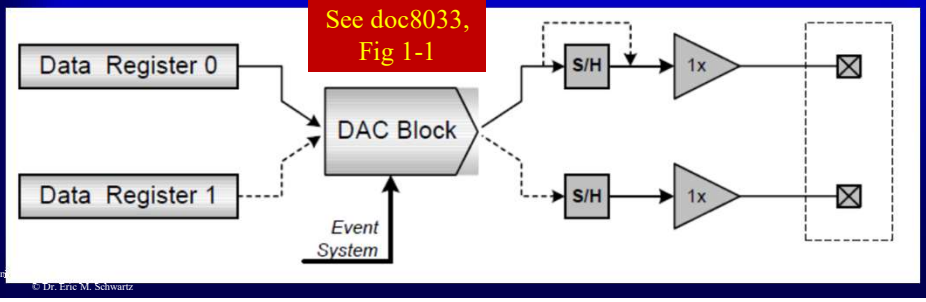
XMEGA DAC Features

- 12-bit resolution
- Up to 1M conversions/sec per channel
  - >Two independent channels (on each of Port A & B)
- Continuous drive or sample-and-hold output
- Internal and external reference options
- Event system and DMA can activate DAC

See doc8033

See doc8331, sec 29

See doc8033, Fig 1-1



3

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DAC Reference and Output Voltages

- The same voltage references used for the ADC are used for the DAC
  - >Internal 1.00V
  - >Internal Vcc/1.6V (=2.0625V for Vcc=3.3V)
  - >Internal Vcc/2V
  - >External voltage at AREF pin on PORTA
  - **>External voltage at AREF pin on PORTB (bits 0 & 1)**
- The output voltages from a DAC channel, V_{DACn}, is given by:
  - > Note the denominator is **not** 2^{12}

$$V_{DACn} = \frac{CHnDATA}{0xFFF} \times VREF$$

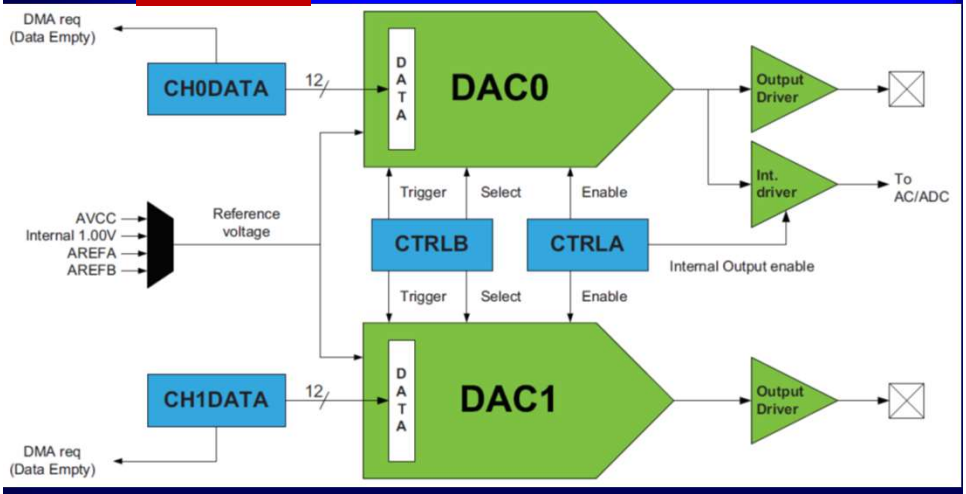
doc8331, §29.5

4

4

EEL 4744 XMEGA DAC Block Diagram

doc8331, Figure 29-1



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EEL 4744 DAC – Control Register A

- ~~**Bit 4 – IDOEN: Internal Output Enable**~~
  - > Setting this bit will enable the internal DAC channel 0 output to be used by the Analog Comparator and ADC. This will then also disable the output pin for DAC Channel 0.
- **Bit 3 – CH1EN: Channel 1 Output Enable**
  - > Setting this bit will make channel 1 available on the output pin.
- **Bit 2 – CH0EN: Channel 0 Output Enable**
  - > Setting this bit will make channel 0 available on the output pin unless IDOEN is set to 1.
- ~~**Bit 1 – LPMODE: Low Power Mode**~~
  - > Setting this bit enables the DAC low-power mode. The DAC is turned off between each conversion to save current. Conversion time will be doubled when new conversions are started in this mode.
- **Bit 0 – ENABLE: Enable**
  - > This bit enables the entire DAC.

Bit	7	6	5	4	3	2	1	0
+0x00	–	–	–	IDOEN	CH1EN	CH0EN	LPMODE	ENABLE
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

DAC_CTRLA

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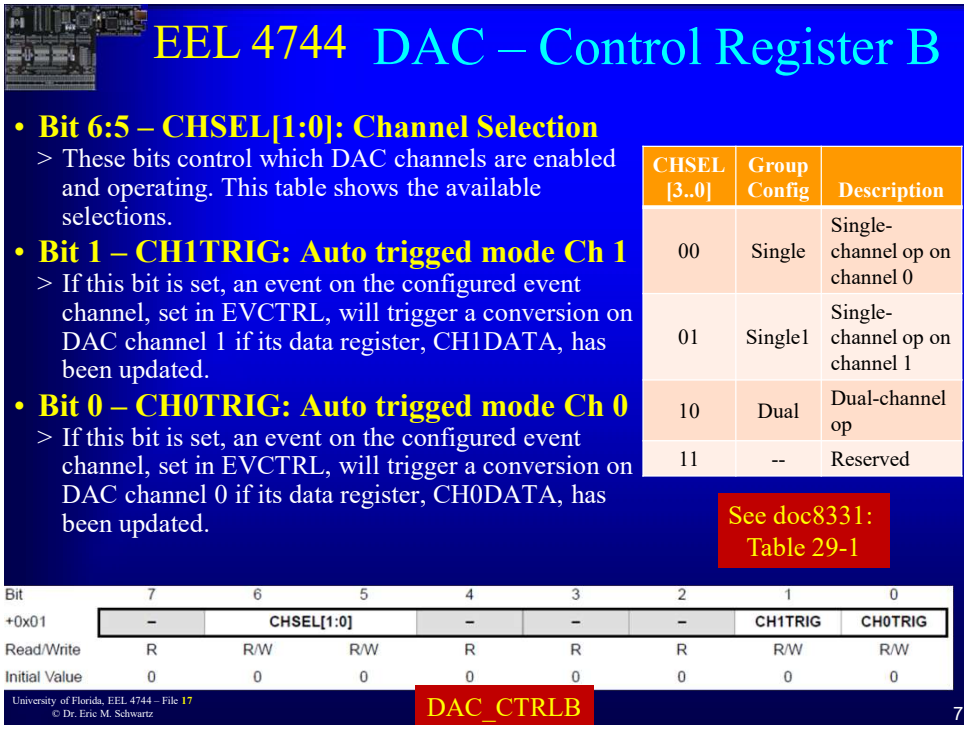
EEL 4744 DAC – Control Register B
• Bit 6:5 – CHSEL[1:0]: Channel Selection
> These bits control which DAC channels are enabled and operating. This table shows the available selections.
• Bit 1 – CH1TRIG: Auto trigged mode Ch 1
> If this bit is set, an event on the configured event channel, set in EVCTRL, will trigger a conversion on DAC channel 1 if its data register, CH1DATA, has been updated.
• Bit 0 – CH0TRIG: Auto trigged mode Ch 0
> If this bit is set, an event on the configured event channel, set in EVCTRL, will trigger a conversion on DAC channel 0 if its data register, CH0DATA, has been updated.
CHSEL [3..0] | Group Config | Description
00 | Single | Single-channel op on channel 0
01 | Single1 | Single-channel op on channel 1
10 | Dual | Dual-channel op
11 | -- | Reserved
See doc8331: Table 29-1
Bit 7 6 5 4 3 2 1 0
+0x01 – CHSEL[1:0] – – – CH1TRIG CH0TRIG
Read/Write R R/W R/W R R R R/W R/W
Initial Value 0 0 0 0 0 0 0 0
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DAC_CTRLB
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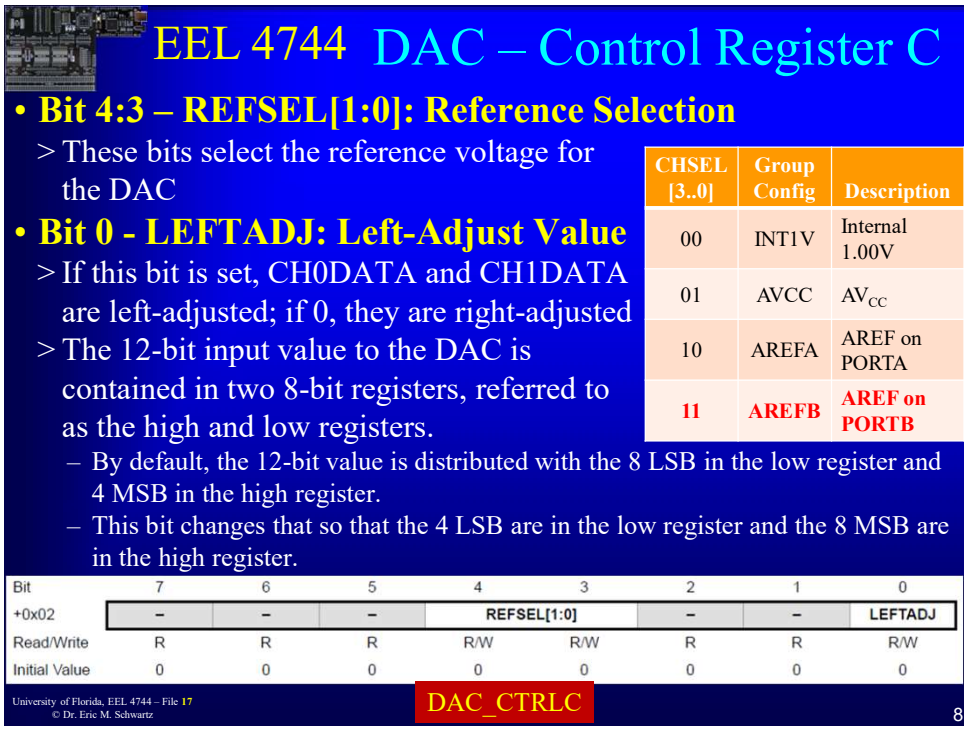
EEL 4744 DAC – Control Register C
• Bit 4:3 – REFSEL[1:0]: Reference Selection
> These bits select the reference voltage for the DAC
• Bit 0 - LEFTADJ: Left-Adjust Value
> If this bit is set, CH0DATA and CH1DATA are left-adjusted; if 0, they are right-adjusted
> The 12-bit input value to the DAC is contained in two 8-bit registers, referred to as the high and low registers.
– By default, the 12-bit value is distributed with the 8 LSB in the low register and 4 MSB in the high register.
– This bit changes that so that the 4 LSB are in the low register and the 8 MSB are in the high register.
CHSEL [3..0] | Group Config | Description
00 | INT1V | Internal 1.00V
01 | AVCC | AVCC
10 | AREFA | AREF on PORTA
11 | AREFB | AREF on PORTB
Bit 7 6 5 4 3 2 1 0
+0x02 – – – REFSEL[1:0] – – LEFTADJ
Read/Write R R R R/W R/W R R R/W
Initial Value 0 0 0 0 0 0 0 0
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DAC_CTRLC
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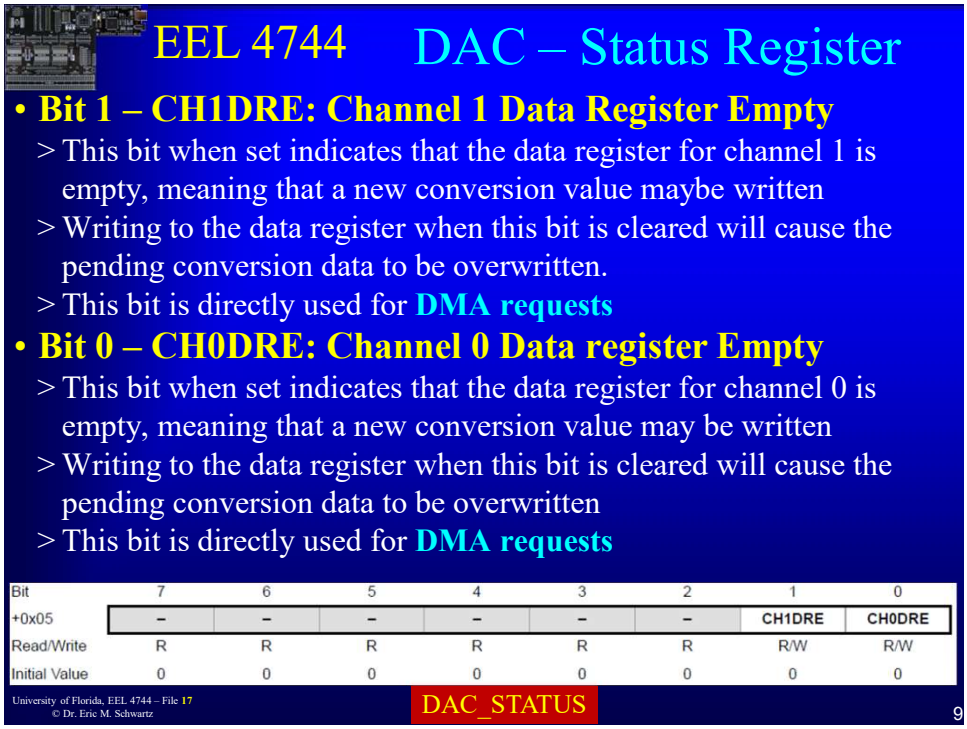
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DAC – Status Register
• Bit 1 – CH1DRE: Channel 1 Data Register Empty
> This bit when set indicates that the data register for channel 1 is empty, meaning that a new conversion value maybe written
> Writing to the data register when this bit is cleared will cause the pending conversion data to be overwritten.
> This bit is directly used for DMA requests
• Bit 0 – CH0DRE: Channel 0 Data register Empty
> This bit when set indicates that the data register for channel 0 is empty, meaning that a new conversion value may be written
> Writing to the data register when this bit is cleared will cause the pending conversion data to be overwritten
> This bit is directly used for DMA requests
Bit 7 6 5 4 3 2 1 0
+0x05 – – – – – – CH1DRE CH0DRE
Read/Write R R R R R R R/W R/W
Initial Value 0 0 0 0 0 0 0 0
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DAC_STATUS
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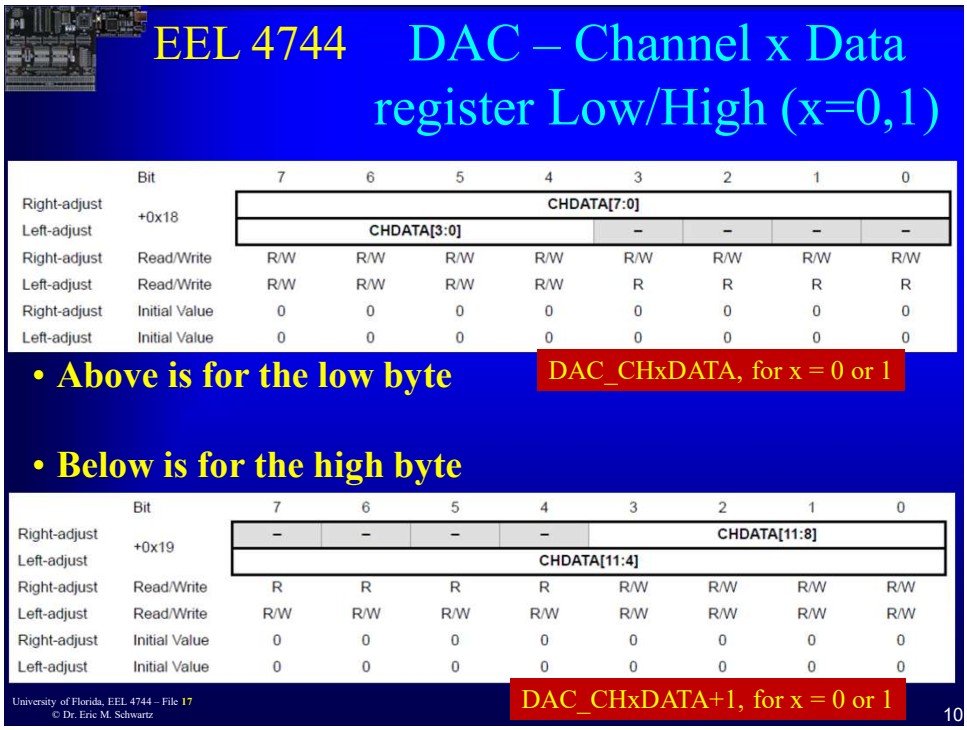
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DAC – Channel x Data register Low/High (x=0,1)
Bit 7 6 5 4 3 2 1 0
Right-adjust +0x18 CHDATA[7:0]
Left-adjust CHDATA[3:0] – – – –
Right-adjust Read/Write R/W R/W R/W R/W R/W R/W R/W R/W
Left-adjust Read/Write R/W R/W R/W R/W R R R R
Right-adjust Initial Value 0 0 0 0 0 0 0 0
Left-adjust Initial Value 0 0 0 0 0 0 0 0
• Above is for the low byte
DAC_CHxDATA, for x = 0 or 1
• Below is for the high byte
Bit 7 6 5 4 3 2 1 0
Right-adjust +0x19 – – – – CHDATA[11:8]
Left-adjust CHDATA[11:4]
Right-adjust Read/Write R R R R R/W R/W R/W R/W
Left-adjust Read/Write R/W R/W R/W R/W R/W R/W R/W R/W
Right-adjust Initial Value 0 0 0 0 0 0 0 0
Left-adjust Initial Value 0 0 0 0 0 0 0 0
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DAC_CHxDATA+1, for x = 0 or 1
10

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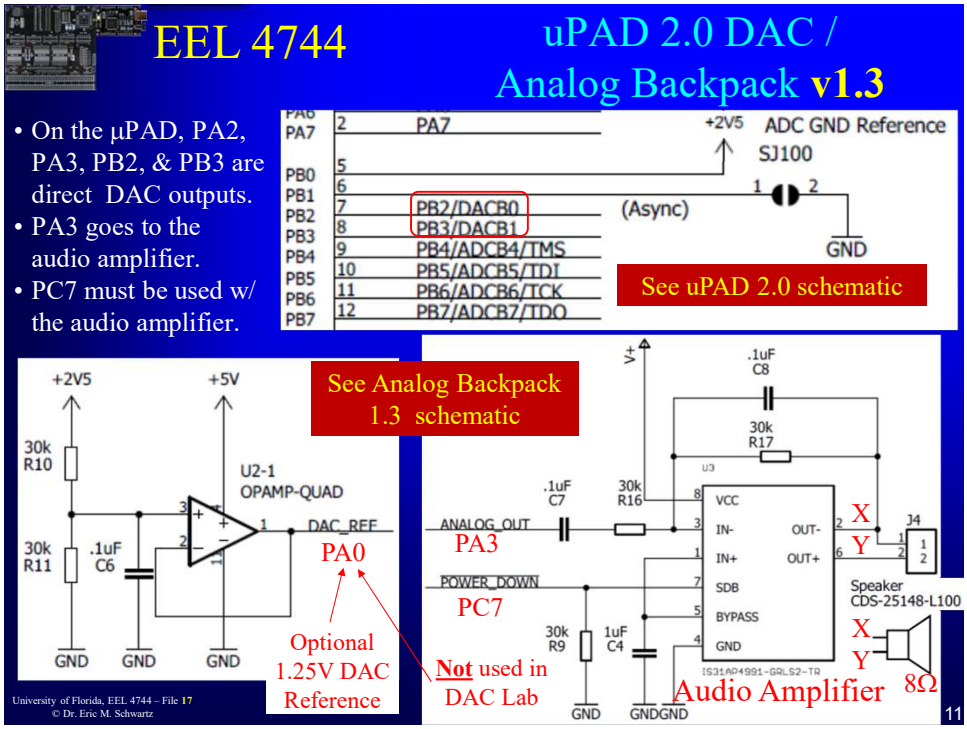
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uPAD 2.0 DAC / Analog Backpack v1.3
• On the µPAD, PA2, PA3, PB2, & PB3 are direct DAC outputs.
• PA3 goes to the audio amplifier.
• PC7 must be used w/ the audio amplifier.
PA7
PB2/DACB0
PB3/DACB1
PB4/ADCB4/TMS
PB5/ADCB5/TDI
PB6/ADCB6/TCK
PB7/ADCB7/TDO
+2V5
ADC GND Reference
SJ100
(Async)
GND
See uPAD 2.0 schematic
See Analog Backpack 1.3 schematic
+2V5
+5V
30k R10
30k R11
.1uF C6
U2-1 OPAMP-QUAD
DAC_REF
PA0
Optional 1.25V DAC Reference
.1uF C8
30k R17
.1uF C7
30k R16
ANALOG_OUT
PA3
POWER_DOWN
PC7
VCC
IN-
IN+
SDB
BYPASS
GND
OUT-
OUT+
J4
Speaker CDS-25148-L100
30k R9
1uF C4
Not used in DAC Lab
Audio Amplifier
8Ω
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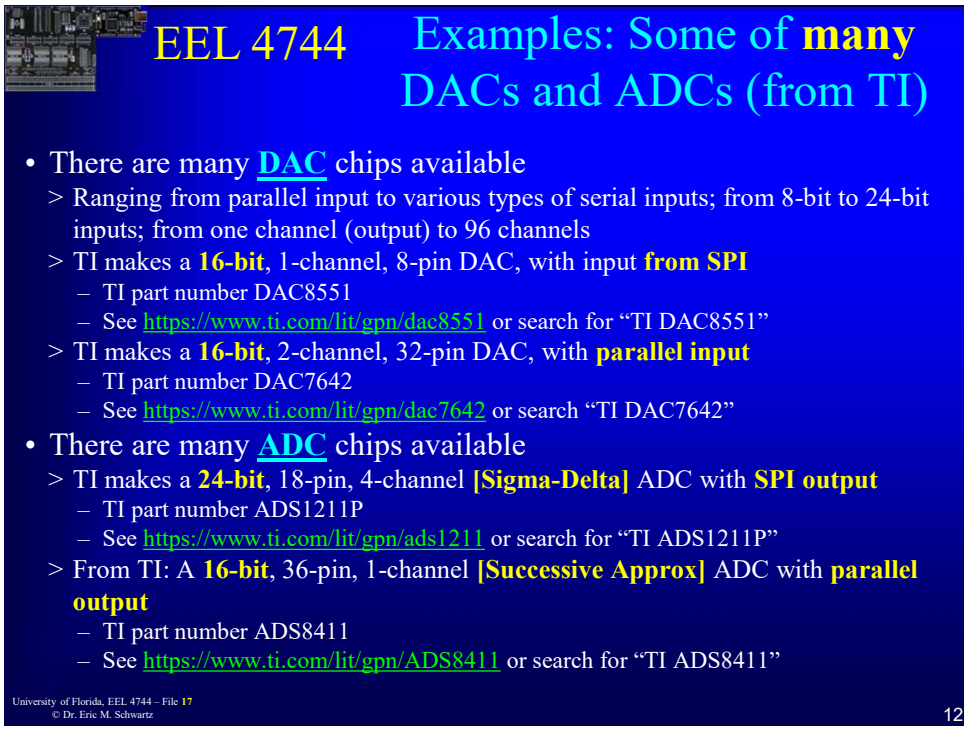
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Examples: Some of many DACs and ADCs (from TI)
• There are many DAC chips available
> Ranging from parallel input to various types of serial inputs; from 8-bit to 24-bit inputs; from one channel (output) to 96 channels
> TI makes a 16-bit, 1-channel, 8-pin DAC, with input from SPI
– TI part number DAC8551
– See https://www.ti.com/lit/gpn/dac8551 or search for "TI DAC8551"
> TI makes a 16-bit, 2-channel, 32-pin DAC, with parallel input
– TI part number DAC7642
– See https://www.ti.com/lit/gpn/dac7642 or search "TI DAC7642"
• There are many ADC chips available
> TI makes a 24-bit, 18-pin, 4-channel [Sigma-Delta] ADC with SPI output
– TI part number ADS1211P
– See https://www.ti.com/lit/gpn/ads1211 or search for "TI ADS1211P"
> From TI: A 16-bit, 36-pin, 1-channel [Successive Approx] ADC with parallel output
– TI part number ADS8411
– See https://www.ti.com/lit/gpn/ADS8411 or search for "TI ADS8411"
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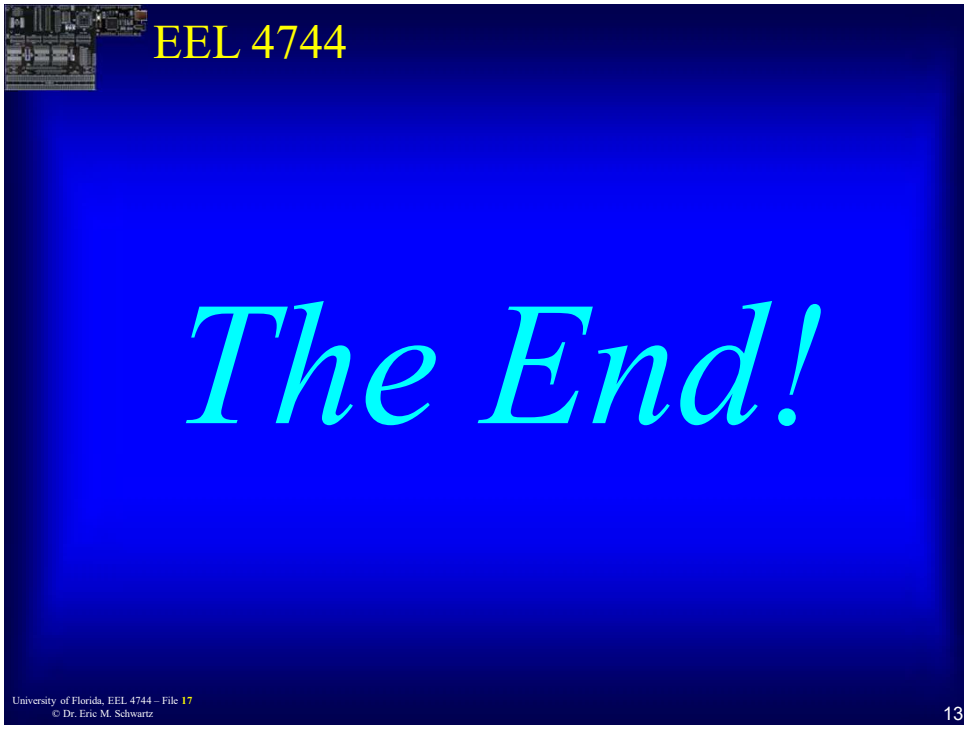
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The End!
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